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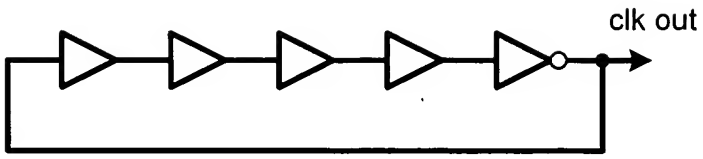

FIG. 1

PRIOR ART

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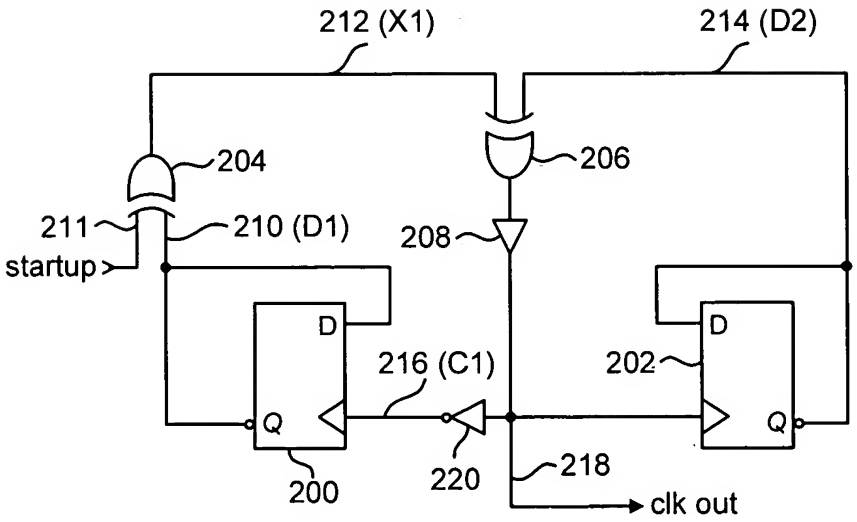

Clock Oscillator Circuit

FIG. 2

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State	D1	Startup	X1	D2	Clk out	C1
0	1	1	0	0	0	1
1	1	0	1	0	1	0
2	1	0	1	1	0	1
3	0	0	0	1	1	0
4	0	0	0	0	0	1
5	1	0	1	0	1	0

FIG. 3